Proposal for Short Term Training
On
FPGA based Digital System Design
Date of commencement: 20th June 2024

The School of Electronics Engineering going to organise a 4 weeks summer training program on FPGA based Digital System Design using Verilog HDL. A Hardware Description Language (HDL) called Verilog is used to simulate and create digital systems. Verilog is used in electronic design for test analysis, timing analysis, logic synthesis, and simulation-based verification. The focus of this course is on developing a thorough understanding of Verilog concepts. The course blends informative lectures with hands-on activities to help students remember fundamental ideas.

Duration: 4 weeks(40hr) + Project
Course Fee: Rs. 5000/-(inclusive all taxes)
Eligibility: B. TECH. 2nd Year or 3rd year
Mode: Hybrid Mode (Theory will be in online mode and hands-on in offline mode in university campus)

Course objectives:
- To learn IEEE standard Verilog HDL and its different modeling styles to model digital circuits.
- To apprehend the concept of delays, test benches and timing checks in digital circuits.
- To understand the fundamentals of FPGAs.
- To perceive the essentials of FPGA based implementation of digital circuits.

Course Outcomes:
The students will be able to:
- Design, simulate and synthesize the digital circuits with Verilog.
- Design combinational and sequential logic circuits.
- Synthesize logic and state machines using automatic logic synthesis program.
- Run a timing and Power calculations
- Use enhanced Verilog file I/O capability.

Week-1:
Introduction to VLSI Design and Verilog HDL:
- VLSI and ASIC Design Flow,
- Basic Concepts of Verilog HDL,
- Modelling: - data flow modelling, Gate level Modelling, Structural Modelling, Behavioural Modelling.
- Test bench and writing a testbench to verify a design

Week-2
- Combination circuit and sequential circuit design using Verilog and their verification.
- Multiplexed seven segment display implementations in FPGA and verify it.
- Interfacing Temperature sensor and displaying its value using FPGA.

Week-3
- Design and implementation of 8-bit signed multiplier using Radix-4 Booth algorithm.
- Implementation of 5-tap FIR filter with ADC and DAC in FPGA.
- Implementation of PWM based stepper motor controller in FPGA.

Week-4:
- Timing verification of a Logic in FPGA.
- FPGA Debugging using Integrated Logic Analyser.
- RTL to layout using Opensource tools.
- A small prject
- Feedback collection

Note:
- The seats are limited and students are allowed to participate on first come first serve basis.
- Minimum attendance of 75% is required to get soft copy of certificate.

Instructor:

Dr. J. K. Das
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